Claims

1. A method of processing first and second successions of data words, each data word including multiple payload data bits, a data block bit (C) and a block character (SOB) having a first state to indicate start of a sequence of data block bits and otherwise having a second state, said method comprising:

detecting as a first event occurrence of the block character of the first succession of data words in the first state and as a second event the next succeeding occurrence of the block character of the second succession of data words in the first state, wherein the second event is delayed by a time Tz relative to the first event,

reading the data block bits from successive data words of the first succession and generating a succession of delayed data block bits of the first succession of data words, delayed by said time Tz relative to the payload data bits of the first succession of data words, and

inserting the data block bits of the delayed succession of data block bits in successive words of the first succession of data words, so that the start of the sequence of data block bits in the first succession of data words coincides with the start of the sequence of data block bits in the second succession of data words.

2. A method according to claim 1, comprising loading a data word of the first succession of data words into a first register, loading a data word of the second succession of data words into a second register, and reading the data words from the first and second registers respectively and combining them to form a single frame of a composite data stream, and wherein the step of detecting the first and second events comprises testing the contents of the first and second registers to detect whether either register contains the block character in the first state.

3. A method according to claim 1, comprising receiving first and second data streams each composed of a succession

of frames, each frame including first and second subframes, wherein each subframe includes multiple payload data bits and a data block bit, and deriving the data words of the first succession from the subframes of the first data stream and deriving the data words of the second succession from the subframes of the second data stream.

4. A method according to claim 3, comprising detecting the frame frequency of the first data stream by generating a frame frequency signal having a frequency equal to the frame frequency, generating a reference signal at a frequency substantially greater than the frame frequency, and counting the number of periods of the reference signal in one period of the frame frequency signal.

5. A routing switch for connection to a plurality of signal sources each providing a data stream composed of a succession of frames, each frame having first and second subframes, wherein the first subframe includes framing bits and each subframe includes multiple payload data bits and a data block bit, the framing bits having a first state to indicate start of a sequence of data block bits and otherwise having a second state, the succession of first subframes constituting a first channel and the succession of second subframes constituting a second channel, and the routing switch including:

a plurality of input modules having respective input terminals for connection to the signal sources,

a plurality of output modules each having an output terminal for connection to a signal destination, and

a routing core for supplying selectively a channel of a first data stream and a channel of a second data stream to any selected output module for combination to provide the output data stream,

and wherein each output module includes a circuit which selectively delays the data block bits of one channel to bring the data block bits of the one channel into phase alignment with the data block bits of the other channel.

6. A method of processing first and second data streams each composed of a succession of frames, each frame having first and second subframes, the succession of first subframes constituting a first channel and the succession of second subframes constituting a second channel, wherein each subframe includes multiple payload data bits and a data block bit and the first subframe includes a framing character having a first state to indicate start of a sequence of data block bits and otherwise having a second state, said method comprising:

(a) composing an output data stream from a channel of the first data stream and a channel of the second data stream, and

(b) delaying the data block bits of one channel relative to the payload data bits of the one channel to bring the data block bits of the one channel into phase alignment with the data block bits of the other channel.

7. A method according to claim 6, wherein step (a) includes:

(i) decomposing each subframe of the first data stream to generate a pair of subframe words, wherein each subframe word includes a start bit having a first state to indicate start of a sequence of data block bits and otherwise having a second state,

(ii) decomposing each subframe of the second data stream to generate a pair of subframe words, wherein each subframe word includes a start bit having a first state to indicate start of a sequence of data block bits and otherwise having a second state, and

(iii) extracting one subframe word of each pair generated in step (i) and extracting one subframe word of each pair generated in step (ii),

and step (b) includes:

(i) testing the start bits of the extracted subframe words to identify the start of each sequence of data block bits,

(ii) measuring time delay between occurrence of the

start bit of said other channel in said first state and occurrence of the start bit of said one channel in said first state, and

(iii) delaying the data block bits of said one channel by said time delay.